

REMARKS

Enclosed herewith is a Substitute Specification in which the specification as filed has been amended in various places to correct typographical and grammatical errors.

In support of the above, enclosed herewith is a copy of the specification as filed marked up with the above changes.

The undersigned attorney asserts that no new matter has been incorporated into the Substitute Specification.

The claims have been amended to more clearly define the invention as disclosed in the written description. In particular, claim 4 has been made dependent on claim 3, while claim 7 has been made dependent on claim 2. In addition, the claims have been amended for clarity.

Applicant believes that the above changes answer the Examiner's 35 U.S.C. 112, paragraph 2, rejection of the claims, and respectfully requests withdrawal thereof.



PHOENIX 000387

AGC CIRCUIT

BACKGROUND OF THE INVENTION

Field Of The Invention

[0001] The invention relates to an automatic gain control (AGC) circuit comprising a ~~digitally-digitally~~-controlled amplifier ~~being provided with~~having a gain control loop including a level detector, a threshold circuit and a digital gain control signal generator ~~being coupled to a gain control input of the digitally controlled amplifier for supplying thereto,~~ a digital gain control signal, as well as to a digital audio broadcast (DAB) receiver comprising such an AGC circuit.

Description Of The Related Art

[0002] An AGC circuit of this kind is ~~on itself widely known,~~ e.g., from U.S. ~~patent no.~~ Patent 4 774 474.

15 —————The known AGC provides for an automatic digital gain setting of the ~~digitally-digitally~~-controlled amplifier, such that the output signal is stabilized at a particular predetermined level. The ~~digitally-digitally~~-controlled amplifier may comprise a number of gain stages in series and/or parallel, which can be

20 switched off and on, ~~dependent~~-depending on the gain setting required to stabilize the output signal level. Each gain stage can be optimized for linearity, ~~signal-signal-to-to~~-noise ratio and gain within its working area. This allows ~~to optimize~~optimization

of the ~~digitally-digitally~~-controlled amplifier at small input signal amplitudes for proper ~~signal-signal-to-to~~-noise ratio at high gain factor. The ~~digitally-digitally~~-controlled amplifier can be optimized at large input signal amplitudes for accurate
5 linearity and low gain factor.

[0003] However, small deviations around the switching levels of the known digital gain control signal give rise to repeated switching between two gain settings. This modulates the output signal of the ~~digitally-digitally~~-controlled amplifier, ~~therewith~~
10 ~~thereby~~ causing an increase in the bit error rate, which may cause, e.g., audible distortions to occur.

SUMMARY OF THE INVENTION

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[0004] Therefore, it is an object of the invention to stabilize the gain setting and to avoid said repeated switching between gain settings.

[0005] An AGC circuit comprising a ~~digitally-digitally~~-
20 controlled amplifier ~~being provided with~~having a gain control loop including a level detector, a threshold circuit and a digital gain control signal generator being coupled to a gain control input of the ~~digitally-digitally~~-controlled amplifier for supplying ~~thereto~~ a digital gain control signal, according to the invention is,
25 therefore, characterized ~~by~~ in that the AGC circuit further

comprises a ~~continuously~~-~~continuously~~-controlled amplifier being coupled between an output of the ~~digitally~~-~~digitally~~-controlled amplifier and the level detector, an output of the level detector being coupled to a gain control input of the ~~continuously~~
5 ~~continuously~~-controlled amplifier for supplying thereto ~~ana~~ continuous gain control signal, the gain variation range of the ~~continuously~~-~~continuously~~-controlled amplifier at least corresponding to the gain step variation of the ~~digitally~~
10 ~~digitally~~-controlled amplifier at an incremental step of said digital gain control signal.

[0006] By applying the measure according to the invention, a course gain setting is obtained with the ~~digitally~~-~~digitally~~-controlled amplifier, whereas a continuous gain setting is obtained with the ~~continuously~~-~~continuously~~-controlled amplifier. By
15 choosing the gain variation range of the ~~continuously~~-~~continuously~~-controlled amplifier to correspond at least to the gain step variation of the ~~digitally~~-~~digitally~~-controlled amplifier at an incremental step of said digital gain control signal, repeated switching between gain settings are avoided.

20 [0007] To stabilize the gain loop against oscillation, the AGC circuit further comprises, preferably, a loop filter is being coupled between the output of the level detector, on the one hand, and the gain control input of the ~~continuously~~-~~continuously~~-controlled amplifier and the threshold circuit, on the other hand.

[0008] A further preferred embodiment of the AGC circuit, allowing for a cost-effective implementation, is characterized in that the threshold circuit comprises first and second comparators for comparing the output signal of the level detector with positive and negative threshold levels around a zero level for initiating the digital gain control signal generator for a stepwise variation of the gain of the ~~digitally-digitally~~-controlled amplifier.

[0009] Preferably, the digital gain control signal generator comprises a pulse generator coupled to a clock-signal input of a digital counter for supplying a clock-signal thereto, the threshold circuit including a third comparator for comparing the output signal of the level detector with a zero level, and an output of the third comparator being coupled to an up/down input of the counter.

[0010] Another preferred embodiment of the AGC circuit according to the invention, is characterized in that the gain variation range of the ~~continuously-continuously~~-controlled amplifier, caused defined by the range of the continuous gain control signal between the negative and positive threshold levels, corresponds at least to a gain variation of the ~~digitally-digitally~~-controlled amplifier exceeding the value for one incremental step, preferably over two or more consecutive incremental steps, of said digital gain control signal. This further secures the prevention of repeated switching between two gain settings.

[0011] A receiver for digitally modulated signals, for example, a digital audio broadcast (DAB) receiver, comprising an AGC circuit according to the invention is characterized ~~by~~ in that said ~~digitally-digitally-controlled~~ amplifier ~~being~~ is coupled between
5 an RF input filter and a phase quadrature mixer stage, phase quadrature outputs thereof being coupled through frequency selective means to a pair of phase quadrature ~~continuously~~ continuously-controlled amplifiers, this pair of phase quadrature ~~continuously-controlled~~ amplifiers being coupled
10 through to a pair of phase quadrature ~~analogue-analog-to-to~~-digital converters to said level detector.

BRIEF DESCRIPTION OF THE DRAWINGS

15 [0012] The invention will now be described with reference to the accompanying drawings, in which:

[0013] Figure 1 shows a preferred embodiment of an AGC circuit according to the invention; and

[0014] Figure 2 shows a preferred embodiment of a DAB receiver
20 using an AGC circuit according to the invention.

[0015] The figures are not drawn to scale. In general, like reference numerals refer to like parts.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0016] Figure 1 shows a preferred embodiment of an automatic gain control (AGC) circuit according to the invention comprising a ~~digitally-digitally-controlled~~ amplifier DCA followed by a ~~continuously-continuously-controlled~~ amplifier VCA, an output thereof being coupled to a gain control loop including, subsequently, a level detector LD and a loop filter LF. An output of the loop filter LF is coupled to a gain control input of the ~~continuously-continuously-controlled~~ amplifier VCA for supplying thereto an continuous gain control signal, as well as to a threshold circuit T. A first output TO1 of the threshold circuit T is coupled, via a pulse generator PG, to a clock signal input CI of a digital counter C, and a second output TO2 of the threshold circuit T is coupled to an up/down control input U/D of said digital counter C. The digital counter C supplies a digital gain control signal to the ~~digitally-digitally-controlled~~ amplifier DCA. The pulse generator PG and said digital counter C therewith function as a digital gain control signal generator.

20 [0017] The gain variation range of the ~~continuously~~ continuously-controlled amplifier VCA corresponds at least to the gain step variation of the ~~digitally-digitally-controlled~~ amplifier DCA at an incremental step of said digital gain control signal.

[0018] The threshold circuit T comprises first to third comparators T1 - T3, the first and second comparators T1 and T2 are

being used to compare the output signal of the loop filter LF, respectively, with positive and negative threshold levels V_{tp} and V_{tn} around a zero level V_0 , and the third comparator T3 ~~is being~~ used to compare the output signal of the level detector with a zero level. Therefore, the first to third comparators T1 - T3 are each provided with positive and negative inputs, said positive inputs being coupled in common to the output of the loop filter LF, the negative inputs of the first and second comparators T1 and T2 being coupled, through respective positive and negative threshold voltage sources $V_{tp} = +\Delta V$ and $V_{tn} = -\Delta V$, to ~~mass-ground~~, and the negative input of the third comparator T3 being coupled, through a zero voltage source (current source), to ~~massground~~. Outputs of the first and second comparators T1 and T2 are coupled, through an OR-gate OR, to the first output T01 of the threshold circuit T, an output of the third comparator T3 being coupled, via the second output T02 of the threshold circuit T, to the up/down control input U/D of the digital counter C.

[0019] If the output signal of the loop filter LF increases above the positive threshold level V_{tp} , then the first comparator T1 causes the pulse generator GP to generate and supply a clock pulse to the counter C. If the output signal of the loop filter LF decreases below the negative threshold level V_{tn} , then the second comparator T2 causes the pulse generator GP to generate and supply a clock pulse to the counter C. The third comparator T3 controls the digital counter C to count down at the reception of a clock

pulse from the pulse generator PG when the output signal of the loop filter LF increases above the positive threshold level V_{tp} . The third comparator T3 controls the digital counter C to count up at the reception of a clock pulse from the pulse generator PG when
5 the output signal of the loop filter LF decreases below the positive threshold level V_{tn} . The range between positive and negative threshold levels V_{tp} and V_{tn} defines the range in which the output signal of the loop filter LF, i.e., the continuous gain control signal for the ~~continuously~~ continuously-controlled
10 amplifier VCA, may vary without ~~for~~ changing the gain setting of the ~~digitally~~ digitally-controlled amplifier DCA.

[0020] By choosing, in accordance with the invention, the gain variation range of the ~~continuously~~ continuously-controlled
15 amplifier VCA to correspond at least to the gain step variation of the ~~digitally~~ digitally-controlled amplifier DGA at an incremental step of said digital gain control signal, i.e., the gain increase occurring in the ~~digitally~~ digitally-controlled amplifier DGA at an up-count of one clock-pulse and/or the gain decrease occurring at a
20 down-count of one clock-pulse, astable gain settings of the ~~digitally~~ digitally-controlled amplifier DGA are avoided.

[0021] Preferably, the gain variation range of the ~~continuously~~ continuously-controlled amplifier VCA is chosen to correspond to a gain variation of the ~~digitally~~ digitally-controlled amplifier DGA
25 exceeding the value for one incremental step, preferably, over two

or more incremental steps, of said digital gain control signal. This further secures the avoidance of repeated switching of the gain of the ~~digitally~~ digitally-controlled amplifier DGA between two gain settings.

5 [0022] However, overshoot in the gain control of the ~~digitally~~ digitally-controlled amplifier ~~DGA-DCA~~ by superposition of subsequent gain step variations may occur, when the time between two consecutive clock-pulses decreases below a certain value, which is defined by the time-constant of the AGC loop. This can be
10 prevented by appropriately limiting the speed of the pulse generator PG.

[0023] Furthermore, the time-constant of the loop filter LF is chosen sufficiently large to prevent regenerative feedback of the gain control signal of the ~~continuously~~ continuously-controlled
15 amplifier VCA.

[0024] Figure 2 shows a preferred embodiment of a DAB receiver using an AGC circuit according to the invention, comprising the ~~above~~ above-mentioned ~~digitally~~ digitally-controlled amplifier DCA ~~being~~ coupled between an RF input filter RF and a phase quadrature
20 mixer stage 1. Phase quadrature outputs of the phase quadrature mixer stage 1 are coupled through phase quadrature frequency selective means 3 to a ~~continuously~~ continuously-controlled phase quadrature amplifier VCA. This ~~continuously~~ continuously-controlled phase quadrature amplifier VCA is coupled through a pair of
25 blocking capacitors 4 to a phase quadrature ~~analogue~~ analog-~~to-to-~~

digital converter 5. Outputs of the phase quadrature ~~analogue~~
~~analog-to-to-digital~~ converter 5 are coupled through a phase
quadrature decimation filter 8 to a CORDIC mixer 8, followed by a
phase quadrature DAB channel filter 9. Phase quadrature outputs of
5 the phase quadrature DAB channel filter 9 are coupled through an
~~AGC-AGC-controlled~~ phase quadrature amplifier 10 to phase
quadrature inputs of a Fast Fourier Transform device 12, a signal
output thereof supplying a ~~wanted~~-desired base-band DAB modulation
signal, a first control output thereof supplying a frequency
10 control signal to the CORDIC demodulator 8, and a second control
output thereof supplying a time synchronization signal to a clock-
signal generator 6. The clock-signal generator 6 supplies a clock-
signal to the phase quadrature ~~analogue~~-~~analog-to-to-digital~~
converter 5.

15 [0025] The signal processing of a DAB receiver as provided by
the circuitry 1-12 is on itself known, e.g., from U.S. ~~patent~~
~~no.~~-Patent 6,021,165. For a proper understanding of the present
invention, detailed knowledge thereof is not required. For this
reason, no further details with regard to said DAB receiver
20 circuitry will be given.

[0026] In the DAB receiver as shown in this Figure 2, the
~~digitally-digitally-controlled~~ amplifier DCA functions as a
broadband amplifier, whereas the ~~continuously-continuously-~~
controlled phase quadrature amplifier VCA is functioning as a
25 ~~narrow-narrow-band~~ amplifier. The level of the phase quadrature

output signal of the ~~continuously~~ continuously-controlled phase quadrature amplifier VCA is detected at two specific locations in the phase quadrature receiver signal path, namely, at the output of the phase quadrature frequency selective means 9 and at an output of the phase quadrature ~~analogue~~ analog-to-digital converter 5. The level detector LD combines these two level informations into a single gain control signal reflecting, properly, the level of the phase quadrature output signal of the ~~continuously~~ continuously-controlled phase quadrature amplifier VCA.

[0027] Preferably, the AGC circuit according to the invention is applied in receivers for digitally modulated signals, like DAB, GSM, DCS, UMTS, DECT, Bluetooth, etc., which are relatively insensitive to level changes by steps during reception.

[0028] The AGC circuit used in the DAB receiver as shown corresponds in its operation with the one described under ~~figure~~ Figure 1.

[0029] It should be apparent that various changes may be made in the present invention as presented in ~~figures~~ Figures 1 and 2 without departing from the spirit and scope of the invention.

ABSTRACT+ OF THE DISCLOSURE

An automatic gain control (AGC) circuit ~~comprising~~
includes a ~~digitally-digitally~~-controlled amplifier ~~being provided~~
5 ~~with~~having a gain control loop including a level detector, a
threshold circuit and a digital gain control signal generator ~~being~~
coupled to a gain control input of the ~~digitally-digitally~~-
controlled amplifier for supplying thereto a digital gain control
signal. To prevent astable gain settings of the ~~digitally~~
10 ~~digitally~~-controlled amplifier from occurring, a ~~continuously~~
~~continuously~~-controlled amplifier is ~~being~~-coupled between an
output of the ~~digitally-digitally~~-controlled amplifier and the
level detector, an output of the level detector being coupled to a
gain control input of the ~~continuously-continuously~~-controlled
15 amplifier for supplying thereto ~~an~~-a continuous gain control
signal, the gain variation range of the ~~continuously-continuously~~-
controlled amplifier at least corresponding to the gain step
variation of the ~~digitally-digitally~~-controlled amplifier at an
incremental step of ~~said the~~ digital gain control signal.


20

~~Figure 1~~



Applicant believes that this application, containing claims 1-9, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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